CLAIMS

What is claimed is:

1. A method comprising:

receiving a data structure representing a behavior of a circuit element, said circuit element being sequential and said data structure being defined in a hardware description language (HDL) using a specific format;

generating a conversion matrix from the data structure, said conversion matrix to represent the behavior of the circuit element in a generic format; and

determining a generic HDL register and a plurality of generic HDL input logic for the generic HDL register to replicate the behavior represented by the data structure based on the conversion matrix.

2. The method of claim 1 wherein the HDL is Verilog, the data structure is a user defined primitive (UDP), and the generic HDL register and the generic HDL input logic consist entirely of Verilog primitives.

3. The method of claim 1 wherein the specific format comprises a technology-specific format used to create a library of elements from which the circuit element is received.

4. The method of claim 1 wherein the conversion matrix comprises a plurality of entries representing every state of the circuit element and every corresponding next state of the circuit element.

5. The method of claim 1 wherein generating the conversion matrix comprises:

performing a reachability analysis on the conversion matrix to classify whether each particular state of the circuit element defined by the conversion matrix is reachable.

6. The method of claim 1 wherein generating the conversion matrix comprises:

identifying input signals and an output signal of the circuit element from the data structure;

evaluating state transitions for the circuit element by evaluating the data structure for a next output signal for each transition of the input signals and for each current output signal; and

populating entries of the conversion matrix for each state transition.

7. The method of claim 6 wherein states for individual signals comprise 0, 1, and X.

8. The method of claim 1 wherein the conversion matrix is organized into a plurality of current states of the circuit element and corresponding next states of the circuit element, and wherein determining the generic HDL register and the plurality of generic HDL input logic comprises:

classifying each next state of the conversion matrix into one of a plurality of sets of states based on predefined criteria;

selecting either an edge sensitive HDL primitive or a level sensitive HDL primitive for the generic HDL register based on selected ones of the plurality of sets of states;

selecting a particular set of functions based on the generic HDL register selected, each function of the particular set of functions corresponding to an input to the generic HDL register; and

evaluating the particular set of functions to determine the plurality of generic HDL input logic.

9. The method of claim 8 wherein each next state is classified according to level (L) or edge (E) sensitive states, according to reachable or unreachable (UR) states, and according to six categories of output state transitions (QQ+ = 00, 01, 0X, 10, 11, 1X) such that the plurality of sets of states comprises 24 sets (L00, L01, L0X, L10, L11, L1X, E00, E01, E0X, E10, E11, E1X, LUR00, LUR01, LUR0X, LUR10, LUR11, LUR1X, EUR00, EUR01, EUR 0X, EUR10, EUR11, EUR1X).

10. The method of claim 9 wherein each current state comprises N current input values and a current output value Q, wherein each current state is classified as reachable or unreachable, wherein each next state comprises N next input values and a next output value Q+, wherein individual value states comprise one of 0, 1, and X, and wherein classifying each next state comprises:

selecting a particular next state having a particular output value Q+;

identifying any current states corresponding to the particular next state in the conversion matrix to provide identified current states;

ignoring any of the identified current states that have a current input value of X to provide a set of remaining current states;

organizing the remaining current states by their respective output values Q;

classifying the particular next state as a level sensitive state (L) for one or more of the six output state transitions (QQ+) for any value of Q for which N of the remaining current states have a same value Q;

classifying the particular next state as an edge sensitive state (E) for one or more of the six output state transitions (QQ+) for any value of Q for which less than N of the remaining current states have a same value Q; and

classifying the particular next state as unreachable (UR) for one or more of the six output state transitions (QQ+) for any value of Q for which all of the remaining current states are classified as unreachable.

11. The method of claim 9 wherein selecting either the edge sensitive HDL primitive or the level sensitive HDL primitive comprises:

selecting the level sensitive HDL primitive if sets E01 and E10 are empty.

12. The method of claim 9 wherein the particular set of functions for the edge sensitive HDL primitive comprise:

Fset = L01 with do not cares for a union of L11, LUR01, and LUR11;

Frst = L10 with do not cares for a union of L00, LUR10, and LUR00;

Fclen = a single common input identified in sets E01 and E10;

Ftmpa = selected next states from a union of E01, E11, and L11;

Ftmpb = Ftmpa with do not cares for selected next states from a union of EUR01, EUR11, and LUR11;

Fd = Ftmpb with do not cares for a union of Fset and Frst, wherein the single common input identified for Fclen is ignored, and wherein the selected next states are edge states having a same edge transition as the single common input identified for Fclen

13. The method of claim 9 wherein the particular set of functions for the level sensitive HDL primitive comprise:

Fset = L01 with do not cares for L11;

Frst = L10 with do not cares for L00;

Fclen = 0; and

Fd = 0.

14. The method of claim 9 wherein the particular set of functions for the level sensitive HDL primitive comprise:

Fset = 0;

Frst = 0;

Fclen = (L01 with do not cares for L11) union with (L10 with do not cares for L00); and

Fd = L01 with do not cares for L11.

15. The method of claim 9 wherein the particular set of functions for the level sensitive HDL primitive comprise:

Fset = a single input identified from the connectivity matrix for which there is no current state for which the output Q+ of the corresponding next state is one;

Frst = a single input identified from the connectivity matrix for which there is no current state for which the output Q+ of the corresponding next state is zero;

Ftmp1 = L01 with do not cares for a union of L11, LUR01, and LUR11;

Ftmp2 = L10 with do not cares for a union of L00, LUR10, and LUR00;

Fclen = a union of Ftmp1 and Ftmp2 with do not cares for a union of Fset and Frst; and

Fd = Ftmp1 with do not cares for an inverted Fclen.

16. A machine readable medium having stored thereon machine executable instructions to implement a method comprising:

receiving a data structure representing a behavior of a circuit element, said circuit element being sequential and said data structure being defined in a hardware description language (HDL) using a specific format;

generating a conversion matrix from the data structure, said conversion matrix to represent the behavior of the circuit element in a generic format; and

determining a generic HDL register and a plurality of generic HDL input logic for the generic HDL register to replicate the behavior represented by the data structure based on the conversion matrix.

17. The machine readable medium of claim 16 wherein the HDL is Verilog, the data structure is a user defined primitive (UDP), and the generic HDL register and the generic HDL input logic consist entirely of Verilog primitives.

18. The machine readable medium of claim 16 wherein the specific format comprises a technology-specific format used to create a library of elements from which the circuit element is received.

19. The machine readable medium of claim 16 wherein the conversion matrix comprises a plurality of entries representing every state of the circuit element and every corresponding next state of the circuit element.

20. The machine readable medium of claim 16 wherein generating the conversion matrix comprises:

performing a reachability analysis on the conversion matrix to classify whether each particular state of the circuit element defined by the conversion matrix is reachable.

21. The machine readable medium of claim 16 wherein generating the conversion matrix comprises:

identifying input signals and an output signal of the circuit element from the data structure;

evaluating state transitions for the circuit element by evaluating the data structure for a next output signal for each transition of the input signals and for each current output signal; and

populating entries of the conversion matrix for each state transition.

22. The machine readable medium of claim 21 wherein states for individual signals comprise 0, 1, and X.

23. The machine readable medium of claim 16 wherein the conversion matrix is organized into a plurality of current states of the circuit element and corresponding next states of the circuit element, and wherein determining the generic HDL register and the plurality of generic HDL input logic comprises:

classifying each next state of the conversion matrix into one of a plurality of sets of states based on predefined criteria;

selecting either an edge sensitive HDL primitive or a level sensitive HDL primitive for the generic HDL register based on selected ones of the plurality of sets of states;

selecting a particular set of functions based on the generic HDL register selected, each function of the particular set of functions corresponding to an input to the generic HDL register; and

evaluating the particular set of functions to determine the plurality of generic HDL input logic.

24. The machine readable medium of claim 23 wherein each next state is classified according to level (L) or edge (E) sensitive states, according to reachable or unreachable (UR) states, and according to six categories of output state transitions (QQ+ = 00, 01, 0X, 10, 11, 1X) such that the plurality of sets of states comprises 24 sets (L00, L01, L0X, L10, L11, L1X, E00, E01, E0X, E10, E11, E1X, LUR00, LUR01, LUR0X, LUR10, LUR11, LUR1X, EUR00, EUR01, EUR 0X, EUR10, EUR11, EUR1X).

25. The machine readable medium of claim 24 wherein each current state comprises N current input values and a current output value Q, wherein each current state is classified as reachable or unreachable, wherein each next state comprises N next input values and a next output value Q+, wherein individual value states comprise one of 0, 1, and X, and wherein classifying each next state comprises:

selecting a particular next state having a particular output value Q+;

identifying any current states corresponding to the particular next state in the conversion matrix to provide identified current states;

ignoring any of the identified current states that have a current input value of X to provide a set of remaining current states;

organizing the remaining current states by their respective output values Q;

classifying the particular next state as a level sensitive state (L) for one or more of the six output state transitions (QQ+) for any value of Q for which N of the remaining current states have a same value Q;

classifying the particular next state as an edge sensitive state (E) for one or more of the six output state transitions (QQ+) for any value of Q for which less than N of the remaining current states have a same value Q; and

classifying the particular next state as unreachable (UR) for one or more of the six output state transitions (QQ+) for any value of Q for which all of the remaining current states are classified as unreachable.

26. The machine readable medium of claim 24 wherein selecting either the edge sensitive HDL primitive or the level sensitive HDL primitive comprises:

selecting the level sensitive HDL primitive if sets E01 and E10 are empty.

27. The machine readable medium of claim 24 wherein the particular set of functions for the edge sensitive HDL primitive comprise:

Fset = L01 with do not cares for a union of L11, LUR01, and LUR11;

Frst = L10 with do not cares for a union of L00, LUR10, and LUR00;

Fclen = a single common input identified in sets E01 and E10;

Ftmpa = selected next states from a union of E01, E11, and L11;

Ftmpb = Ftmpa with do not cares for selected next states from a union of EUR01, EUR11, and LUR11;

Fd = Ftmpb with do not cares for a union of Fset and Frst, wherein the single common input identified for Fclen is ignored, and wherein the selected next states are edge states having a same edge transition as the single common input identified for Fclen

28. The machine readable medium of claim 24 wherein the particular set of functions for the level sensitive HDL primitive comprise:

Fset = L01 with do not cares for L11;

Frst = L10 with do not cares for L00;

Fclen = 0; and

Fd = 0.

29. The machine readable medium of claim 24 wherein the particular set of functions for the level sensitive HDL primitive comprise:

Fset = 0;

Frst = 0;

Fclen = (L01 with do not cares for L11) union with (L10 with do not cares for L00); and

Fd = L01 with do not cares for L11.

30. The machine readable medium of claim 16 wherein the particular set of functions for the level sensitive HDL primitive comprise:

Fset = a single input identified from the connectivity matrix for which there is no current state for which the output Q+ of the corresponding next state is one;

Frst = a single input identified from the connectivity matrix for which there is no current state for which the output Q+ of the corresponding next state is zero;

Ftmp1 = L01 with do not cares for a union of L11, LUR01, and LUR11;

Ftmp2 = L10 with do not cares for a union of L00, LUR10, and LUR00;

Fclen = a union of Ftmp1 and Ftmp2 with do not cares for a union of Fset and Frst; and

Fd = Ftmp1 with do not cares for an inverted Fclen.

31. An apparatus comprising:

a processor; and

a machine readable storage medium storing thereon machine executable instructions, the processor to execute the machine executable instructions to

receive a data structure representing a behavior of a circuit element, said circuit element being sequential and said data structure being defined in a hardware description language (HDL) using a specific format;

generate a conversion matrix from the data structure, said conversion matrix to represent the behavior of the circuit element in a generic format; and

determine a generic HDL register and a plurality of generic HDL input logic for the generic HDL register to replicate the behavior represented by the data structure based on the conversion matrix.